

YOUHANNA DIMIAN

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Technical Skills

- **Digital Design:** RTL & Logic Design | FSM Design | Synthesis | Static Timing Analysis (STA) | Clock Domain Crossing (CDC) | Hardware Verification | Testbench Development | Waveform Analysis | FPGA | Computer Architecture | Datapath Design
- **Languages & Protocols:** SystemVerilog | Verilog | VHDL | C/C++ | Python | RISC-V Assembly | MATLAB (Simulink) | Bash | SPI | I²C | UART | CAN | Memory-Mapped I/O
- **Hardware:** PCB Design (Schematic Capture & Layout) | Board Bring-up & Debugging | Circuit Design & Analysis | DC-DC Converters | Photonic Integrated Circuit (PIC) Design | Lab Equipment (Oscilloscope, Logic Analyzer, Multimeter)
- **Tools:** cocotb | Verilator | Icarus Verilog | Quartus Prime | Git | GitHub Actions (CI) | Altium Designer | LTspice

Experience

- ASIC Digital Designer** UW-ASIC Design Team Waterloo, ON, CA Aug. 2026 – Present
- Implementing the **Ray Generator** in **SystemVerilog** for TinyTracer, the **first programmable ray-tracing chip** on **Tiny Tapeout**, generating primary camera rays and secondary matte, metal, and glass bounce rays in **16-bit fixed-point**.
 - Designing a **control FSM** that sequences vector macro-ops over a **valid/ready SystemVerilog interface** to a shared **CORDIC/multiplier** execution unit, saving **area** vs. dedicated arithmetic, and integrating a **Galois LFSR** random number generator.
 - Verifying RTL with **cocotb** testbenches against a **Python** reference model, targeting **FPGA** bring-up and the **Sky130 RTL-to-GDS** flow.
- Electrical Design Intern** EXP Global Inc. Markham, ON, CA May 2026 – Aug. 2026
- Designed building electrical systems in **Revit** across **6 projects**, producing power and lighting layouts, panel schedules, and **single-line diagrams** while sizing feeders and equipment using **load and voltage-drop calculations** under fixed code constraints.
 - **Collaborated with architectural and mechanical teams** through **4–6 review cycles per project** to verify designs against **code and specification requirements**, resolving coordination conflicts and incorporating review comments before final release.
- Electrical Engineering Intern** Electric Power Engineers LLC. Waterloo, ON, CA Sep. 2025 – Dec. 2025
- Broke down large electrical networks into **equivalent circuit models**, analyzing impedance paths and current flow across **dozens of fault and operating scenarios** to identify limiting elements and simulate system behavior.
 - Performed **short-circuit (LG, LL, 3-phase)**, voltage ride-through, and steady-state studies in **PSSE**, evaluating **20+ system cases** for voltage, frequency, and power flow while validating models and delivering technical reports.
- Embedded Systems Intern** SkyJack Inc. (Linamar Corp.) Guelph, ON, CA Jan. 2025 – Apr. 2025
- Collected and analyzed **CAN traces** from boom lift systems using PCAN Explorer to **validate thresholds** and maximum values for key controls (drive forward/reverse), identifying **logic mismatches** in system behavior.
 - Generated CAN messages to simulate machine control inputs and used **MATLAB Simulink** to assess response speed and behavior.
 - **Automated** firmware flashing for **5000+ ZAPI inverters** and built **Python** tools using PCAN / IXXAT to verify COM IDs and cross-check CSV data, cutting QA time **by 70%** and preventing critical deployment errors.
- Photonics Research Intern** McMaster University – Eng. Dept. Hamilton, ON, CA July 2023 – Sep. 2023
- Designed **Photonic Integrated Circuit (PIC)** components, including an Archimedean spiral, reducing simulated **bend losses** and improving transmission **bandwidth**, resulting in measurable **efficiency gains** over baseline designs.
 - Evaluated **waveguide geometries, mode profiles, and propagation losses** to optimize PIC layouts for fabrication.
 - Tested multiple lasers and built **MATLAB automation** that halved experimentation time, and authored an SOP for thermistor calibration.

Projects

SPI-Controlled PWM Peripheral (ASIC)

Personal Project

RTL Design, Verilog, SPI, Hardware Verification, cocotb

- Designed an **SPI peripheral** in **Verilog** decoding 16-bit register writes over SCLK/COPI/nCS, using **double-flop synchronizers** and edge detection to safely cross the asynchronous SPI signals into the **system clock domain**.
- Built a **5-register control interface** driving a 16-output PWM peripheral with independent per-bit static/PWM switching, targeted for **Tiny Tapeout (Sky130)**, and verified SPI transactions and PWM timing using **cocotb testbenches in CI**.

4-Bit ALU Design on FPGA

Personal Project

FPGA, Hardware Verification, RTL Design, VHDL

- Designed a modular 4-bit ALU in **VHDL RTL**, including multiplexers, logic units, and a ripple-carry adder.
- Developed **simulation testbenches**, synthesized the design in **Quartus** analyzing **Fmax** and **critical path**, and deployed on Intel MAX10 FPGA validating real-time outputs on LEDs and 7-segment displays.

Traffic Light Controller on FPGA

Personal Project

FSM Design, Functional Verification, FPGA, RTL Design

- Designed a multi-state **Moore FSM** in VHDL for dual-direction traffic control with pedestrian override, implementing **2-DFF synchronizers** and holding registers to safely handle asynchronous inputs and mitigate **metastability**.
- Developed structured **simulation test cases** to verify reset behavior, **state transitions**, timing (1 Hz enable), and edge-case inputs, then validated functionality on FPGA using **waveform analysis** and on-board outputs.

Education

Bachelor of Applied Science (BASc), Electrical Engineering

University of Waterloo

Expected Apr. 2029

- President's Scholarship | **Relevant Courses:** Digital Circuits & Design, Digital Computers, Semiconductor Physics & Devices, Circuits I & II